In re Patent Application of:
MARIAUD ET AL.
Serial No. 09/989,317
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In the Claims:

Claims 1-4 (Cancelled).

5. (Currently amended) A computer system comprising:
a master apparatus; and
a slave apparatus for communicating with said master
apparatus and communicating via a universal serial bus (USB)
protocol, said slave apparatus comprising

a sending/receiving circuit for sending and
receiving binary information to and from said master
apparatus and supplying status signals based thereon,
and for acknowledging and recording a new message only
when a transfer interruption signal is not supplied,

a plurality of state latches and control circuitry
cooperating therewith for receiving the status signals
from said sending/receiving circuit and supplying state
signals of said sending/receiving circuit based
thereon,

a microprocessor for processing applications of
said slave apparatus and also for processing the binary
information received by said sending/receiving circuit,
and

an interruption state latch and a control circuit
cooperating therewith for supplying an interruption
signal to said microprocessor once the end of a message
has been acknowledged and for supplying the transfer

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interruption signal to said microprocessor once the
start of a new message has been acknowledged and
recorded by said sending/receiving circuit when the
microprocessor ~~is unavailable~~ interruption signal is
supplied.

6. (Previously presented) The computer system of Claim
5 wherein said control circuit for controlling said interruption
state latch comprises at least one logic circuit for receiving
the status signals from said sending/receiving circuit and
setting said interruption state latch to a predetermined logic
level to indicate a microprocessor interruption request.

7. (Previously presented) The computer system of Claim
5 wherein said control circuitry for controlling said state
latches prevents the binary information from said
sending/receiving circuit from being written into said plurality
of state latches during receipt of the start of the new message
and during the presence of the interruption signal.

8. (Previously presented) The computer system of Claim
5 wherein said master apparatus comprises a central processing
unit.

9. (Previously presented) The computer system of Claim
5 wherein said slave apparatus comprises a computer peripheral
device.

10. (Previously presented) The computer system of Claim

5 further comprising a cable connecting said master apparatus and said slave apparatus.

        11. (Currently amended) A computer system comprising:

        a master apparatus; and

        a slave apparatus for communicating with said master apparatus and comprising

        a sending/receiving circuit for sending and receiving binary information to and from said master apparatus and supplying status signals based thereon, and for acknowledging and recording a new message only when a transfer interruption signal is not supplied,

        a plurality of state latches and control circuitry cooperating therewith for receiving the status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon,

        a microprocessor for processing applications of said slave apparatus and also for processing the binary information received by said sending/receiving circuit, and

        an interruption state latch for supplying an interruption signal to said microprocessor once the end of a message has been acknowledged and for supplying the transfer interruption signal to said microprocessor once the start of a new message has been acknowledged and recorded by said sending/receiving circuit when

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~~said microprocessor is unavailable~~ <u>the microprocessor
interruption signal is supplied</u>,

said control circuitry for controlling said state
latches preventing the binary information from said
sending/receiving circuit from being written into said
plurality of state latches during receipt of the start
of the new message and during the presence of the
interruption signal.

12. (Previously presented) The computer system of Claim
11 wherein said master apparatus and said slave apparatus
communicate via a universal serial bus (USB) protocol.

13. (Previously presented) The computer system of Claim
11 further comprising at least one logic circuit for receiving
the status signals from said sending/receiving circuit and
setting said interruption state latch to a predetermined logic
level to indicate a microprocessor interruption request.

14. (Previously presented) The computer system of Claim
11 wherein said master apparatus comprises a central processing
unit.

15. (Previously presented) The computer system of Claim
11 wherein said slave apparatus comprises a computer peripheral.

16. (Previously presented) The computer system of Claim
11 further comprising a cable connecting said master apparatus

and said slave apparatus.

17. (Currently amended) A slave apparatus for communicating with a master apparatus via a universal serial bus (USB) protocol, said slave apparatus comprising:

a sending/receiving circuit for sending and receiving binary information to and from the master apparatus and supplying status signals based thereon, and for acknowledging and recording a new message only when a transfer interruption signal is not supplied;

a plurality of state latches and control circuitry cooperating therewith for receiving the status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon;

a microprocessor for processing applications of the slave apparatus and also for processing the binary information received by said sending/receiving circuit; and

an interruption state latch and a control circuit cooperating therewith for supplying an interruption signal to said microprocessor once the end of a message has been acknowledged and for supplying the transfer interruption signal to said microprocessor once the start of a new message has been acknowledged and recorded by said sending/receiving circuit when said microprocessor is unavailable the microprocessor interruption signal is supplied.

18. (Previously presented) The slave apparatus of Claim 17 wherein said control circuit for controlling said interruption state latch comprises at least one logic circuit for receiving the status signals from said sending/receiving circuit and setting said interruption state latch to a predetermined logic level to indicate a microprocessor interruption request.

19. (Previously presented) The slave apparatus of Claim 17 wherein said control circuitry for controlling said state latches prevents the binary information from said microprocessor from being written into said plurality of state latches during receipt of the start of the new message and during the presence of the interruption signal.

20. (Currently amended) A method of processing interruptions in a slave apparatus for communicating with a master apparatus via a universal serial bus (USB) protocol, the method comprising:

sending and receiving binary information to and from the master apparatus via a sending/receiving circuit and supplying status signals based thereon, the sending/receiving circuit acknowledging and recording a new message only when a transfer interruption signal is not supplied;

generating state signals of the sending/receiving circuit based upon the status signals;

processing applications of the slave apparatus and also
processing the binary information received by the
sending/receiving circuit; and

supplying an interruption signal to a microprocessor of
the slave apparatus once the <u>end of a message has been</u>
<u>acknowledged and for supplying the transfer interruption signal</u>
<u>to said microprocessor once the</u> start of a new message has been
acknowledged and recorded by the sending/receiving circuit when
the microprocessor ~~is unavailable~~ <u>interruption signal is</u>
<u>supplied</u>.

21. (Previously presented) The method of Claim 20
wherein supplying the interruption signal comprises setting an
interruption state latch to a predetermined logic level based
upon the status signals to indicate a microprocessor interruption
request.

22. (Currently amended) A method of processing
interruptions in a slave apparatus for communicating with a
master apparatus via a universal serial bus (USB) protocol, the
method comprising:

generating a state signal indicating the end of a
message;

detecting a start of a new message from the master
apparatus and producing a start of message state signal;

~~recording data from the start of the new message;~~

~~acknowledging receipt of the start of the new message;~~

<u>acknowledging and recording the new message if a</u>

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transfer interruption signal is not supplied;

supplying the transfer interruption signal to the microprocessor once the start of a new message has been acknowledged and recorded;

generating a signal indicating completion of recordation of the data from the start of the new message; and

generating an interruption signal for a microprocessor of the slave apparatus in the presence of the state signal indicating the end of the message, the start of message state signal, and the signal indicating completion of recordation of the data from the start of the new message when the microprocessor ~~is unavailable~~ interruption signal is supplied.